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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/362,200	07/28/1999	KAZUO NAKAZATO	2369/23	6555

23838 7590 04/16/2003

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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/362,200	Applicant(s) Nakazato Et.al.
	Examiner Edgardo Ortiz	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *November 19, 2002 and March 7, 2003*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-12, 15-34, 39-47, and 50-58* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-12, 15-34, 39-47, and 50-58* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 21
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to a terminal disclaimer and response to an office action filed November, 19 2002 and an information disclosure statement filed March 7, 2003.

Terminal Disclaimer

1. The terminal disclaimer filed on November 19, 2002 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 5,952,692 has been reviewed and is accepted. The terminal disclaimer has been recorded

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12, 15-34, 39-47 and 50-58 are rejected under 35 U.S.C. § 102 (b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over by Hijiya et.al. (U.S. Patent No. 5,101,249). With regard to Claim 1, Hijiya teaches an electrode structure (11-2), a charge storage node (7) and a lamination structure including an insulating film (8) and a semiconductor film (9), the lamination structure being disposed between the electrode structure and the charge storing node, see figure 1.

The claim also includes the limitation "the *lamination structure having an energy profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height band profile is low, an electric current flowing in the second configuration for the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge is stored on the node in the first configuration.*" This is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Nevertheless, Hijiya teaches a semiconductor structure which meets the claimed limitations of the energy profile and the flow of current, see column 3, lines 60-68, column 4, lines 1-68, column 5, lines 1-68 and column 6, lines 1-8.

With regard to Claim 2, Hijiya teaches a control electrode (9). The limitation "*the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode*". This is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 3, Hijiya teaches a path for charge carriers between source and drain regions (3, 4), a charge storage node (7) and a lamination structure including an insulating film (8) and a semiconductor film (9), the lamination structure being disposed between the electrode structure and the charge storing node. The limitations "*to produce a filed which alters the conductivity of the path*" and " *lamination structure having an energy profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height band profile is low, an electric current flowing in the second configuration for the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge is stored on the node in the first configuration*". These are intended use limitations which do not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 4, Hijiya teaches a control electrode (9). The limitation "*the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode*". This is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 5, Hijiya teaches a source-drain path between source and drain regions (3, 4), a charge storing node (7) and a lamination structure including an insulating film (8) and a

semiconductor film (9), the lamination structure being disposed between the electrode structure and the charge storing node. The limitations "*to produce a filed which alters the conductivity of the path*" and " lamination *structure having an energy profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height band profile is low, an electric current flowing in the second configuration for the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge is stored on the node in the first configuration*". These are intended use limitation which do not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 6, Hijiya teaches a control electrode (9). The limitation "the *energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode*". This is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 7, Hijiya teaches a lamination structure comprising an insulating film (8) and a conductive film (9) of silicon nitride and silicon material, respectively. See column 2, line 64-65 and column 3, lines 48-51.

With regard to Claims 8 and 9, Hijiya teaches a lamination structure comprising an insulating film (8) and a conductive film (9) of silicon nitride and silicon material, respectively. See column 2, line 64-65 and column 3, lines 48-51.

With regard to Claims 10-12, Hijiya teaches a conductive film (9) of silicon material being polysilicon. See column 2, line 64-65.

With regard to Claim 15, Hijiya teaches a charge storage node (7), an electrode structure (11-2) and a barrier structure (8, 9) between the electrode and the charge storage node. The claims also contains the limitation "the *barrier structure providing a variable internal electrostatic barrier potential configurable by an external bias to provide selectively a relatively low barrier height for which charge carriers can pass from the electrode structure to the charge storage node and vice versa to charge and discharge the node, and a relatively high barrier height to store charge carriers on the charge storage node*". This is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 16, the limitation "*wherein the barrier structure includes a region of barrier material providing a barrier component which is narrower and higher than that provide by the internal electrostatic barrier potential*", is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 17, the limitation "*wherein the height of said barrier component is raised and lowered in response to raising and lowering of the height of the barrier provided by the variable internal electrostatic barrier potential*", is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 18, Hijiya teaches a barrier material comprising a material selected from the group consisting of silicon dioxide and silicon nitride, see column 3, lines 48-51.

With regard to Claim 19, the limitation "*wherein the barrier structure includes a further region of barrier material providing a barrier component which is narrower and higher than that provide by the internal electrostatic barrier potential*", is an intended use limitation which does not structurally distinguish the claimed structure from that taught by Hijiya.

With regard to Claim 20, Hijiya teaches a gate (9) to receive an external bias, the limitation "*to configure the barrier between said high and low barrier heights*" is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 21, Hijiya teaches a substrate (1), an array of memory cells configured on the substrate and a plurality of word lines and data lines extending between the cells, inherently taught by the reference since the disclosed structure is related to nonvolatile semiconductor

memory device of the charge-storage type, which include word lines and data lines to process the charge stored, a charge storage node (7), an electrode (11-2) forming part of the data lines and a barrier structure (8, 9) between the electrode and the charge storage node.

The limitation "the *barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node for charging and discharging the node, and a relatively high barrier height to store charge carriers on the charge storage node*", is an intended use limitation which does not distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 22, Hijiya teaches a source drain path between source and drain regions (3, 4) and inherently sense lines coupled to the source-drain paths of the cells and refreshing circuitry responsive to the sense lines, since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type.

With regard to Claim 23, Hijiya teaches a barrier structure formed of crystaline material, see column 2, lines 62-64.

With regard to Claim 24, Hijiya teaches a barrier structure including polycristalline silicon, see column 2, lines 62-64.

With regard to Claim 25, Hijiya teaches a gate (9) to receive an external bias.

With regard to Claim 26, Hijiya teaches a substrate (1), a charge storage node (7) over the substrate, a barrier structure (8, 9) that overlies the charge storage node and the electrode structure (11-2) overlies the barrier structure.

With regard to Claim 27, Hijiya teaches an insulating layer (6) which overlies the charge storage node (7), the barrier structure (8, 9) that and the electrode structure (11-2).

With regard to Claim 28, Hijiya teaches further device features (3, 4) formed in the substrate (1) that underlie the insulating layer (6).

With regard to Claim 29, Hijiya teaches an insulating layer (6) that comprises an oxide (silicon oxide) of the material of the substrate (silicon).

With regard to Claim 30, Hijiya teaches a an insulating layer (10) that extends over side edges of the barrier structure (8, 9) and the charge storage node (7).

With regard to Claim 31, Hijiya teaches a barrier structure (8, 9) that is substantially co-extensive with the charge storage node (7).

With regard to Claim 32, the limitation "*wherein the barrier structure has a material composition that provides an internal relatively high internal electrostatic barrier in the absence of an applied voltage to the electrode structure, whereby the electrostatic barrier can be lowered upon application of the external bias to the electrode structure*", is an intended use limitation which does not structurally distinguish the claimed invention from that taught by Hijiya.

With regard to Claim 33, Hijiya teaches a gate (9) , the limitation "*configured to apply said external bias into the barrier structure selectively to control conduction of charge carriers between the electrode structure and the charge storage node*" is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 34, Hijiya teaches charge storage node (7) that is made of conductive silicon material, see column 2, lines 61-62.

With regard to Claim 35, Hijiya teaches an electrode structure (11-2), a charge storage node (7) and a barrier structure including an insulating film (8) and a semiconductor film (9), so that the barrier structure being disposed between the electrode structure and the charge storing node, see

figure 1. The limitation "*such that the barrier structure presents an internal relatively high electrostatic barrier potential that retains charge on the storage node, the barrier being lowerable by an external voltage applied to the electrode structure to allow charge carriers to flow from the electrode structure to the charge storage node and vice versa, to charge and discharge the node*", is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 36, Hijiya teaches a substrate (1), a charge storage node (7) over the substrate, a barrier structure (8, 9) that overlies the charge storage node and the electrode structure (11-2) overlies the barrier structure.

With regard to Claim 37, Hijiya teaches oxidizing the substrate (1) to form an insulating layer (6), see column 2, lines 54-56.

With regard to Claim 38, Hjiya teaches a memory device (non volatile semiconductor memory device).

With regard to Claims 39-41, Hijiya inherently teaches refresh, reading and writing circuitry since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type.

With regard to Claim 42, Hijiya teaches a barrier structure formed of crystalline material, see column 2, lines 62-64.

With regard to Claim 43, Hijiya teaches a barrier structure including polycristalline silicon, see column 2, lines 62-64.

With regard to Claim 44, Hijiya teaches a gate (9) to, the limitation "to apply said external bias to the barrier structure" is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 45, Hijiya teaches a substrate (1), an array of memory cells configured on the substrate and a plurality of word lines and data lines extending between the cells and reading and writing circuitry, inherently taught by the reference, since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type, which include word lines and data lines to process the charge stored, a charge storage node (7), an electrode (11-2) forming part of the data lines and a barrier structure (8, 9) between the electrode and the charge storage node.

The limitations "*to read the level of charge stored on the charge storage nodes of the cells individually*", "*to write charge onto the charge storage nodes of the cells individually*" and "*the*

barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node for charging and discharging the node, and a relatively high barrier height to store charge carriers on the charge storage node", are intended use limitations which do not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 46, Hijiya teaches an electrically insulating layer (6) on the substrate (1) with the array of memory cells overlying the insulating layer.

With regard to Claim 47, Hijiya teaches a substrate (1) comprising silicon, an insulating layer (6) selected from the group comprising an oxide and a nitride of silicon, the charge storage node (7) formed of a conductive silicon material and the barrier structure having a layer (9) of polycristalline silicon.

With regard to Claim 48, Hijiya teaches providing a substrate (1), forming device features (3, 4) in the substrate, forming an electrically insulating layer (6) on the substrate overlying the device features, forming a charge storage node (7) overlying the insulating layer, forming a barrier

structure (8, 9) so as to overlie the charge storage node and providing an electrode structure (11-2) overlying the barrier structure.

The limitation "*the barrier structure presenting an electrostatic barrier potential that retains charge on the storage node, the barrier being raisable and lowerable by an external voltage applied to the device so as to allow charge transfer to and from the storage node*", is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 49, Hijiya teaches providing a substrate (1), forming a plurality of word lines and a plurality of date lines extending between the cells, and reading and writing circuitry, inherently taught by the reference, since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type, forming a charge storage node (7) overlying the insulating layer, forming a barrier structure (8, 9) so as to overlie the charge storage node and providing an electrode structure (11-2) overlying the barrier structure.

The limitations "*the barrier structure providing an internal electrostatic barrier potential with a relatively high barrier height to store charge carriers on the charge storage node the barrier potential being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height for which carriers can pass between the*

electrode structure and the charge storage node", "*to read the level of charge stored on the charge storage node of the cels individually*" and "*to write charge onto the charge storage nodes of* the cells individually", are intended use limitations which do not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 50, Hijiya teaches a substrate (1), an array of memory cells configured on the substrate and a plurality of word lines and data lines extending between the cells and reading and writing circuitry, inherently taught by the reference, since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type, which include word lines and data lines to process the charge stored, an electrically insulating layer (6) on the substrate, a charge storage node (7), an electrode (11-2) forming part of the data lines and a barrier structure (8) between the electrode and the charge storage node.

The limitations "*to read the level of charge stored on the charge storage nodes of the cells individually*", "*to write charge onto the charge storage nodes of the cells individually*" and "*the barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node for charging and discharging the node, and a relatively high barrier height to store charge carriers on the charge storage node*", are

intended use limitations which do not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 51, Hijiya teaches a substrate (1) that is comprised of silicon and an electrically insulating layer (6) selected from the group comprising an oxide and a nitride of silicon.

With regard to Claim 52, Hijiya teaches a memory node (7) that is formed of a conductive silicon material.

With regard to Claim 53, Hijiya teaches a barrier structure that includes a layer (9) that is formed of polysilicon material.

With regard to Claim 54, Hijiya teaches a gate (9), the limitation "to control the barrier height presented by the barrier structure to a current that flows to and from the memory node", is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 55, the limitation "wherein the current that flows to and from the memory node, flows vertically through the barrier structure", is a functional recitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 56, Hijiya teaches a substrate (1), an array of memory cells configured on the substrate and a plurality of word lines and data lines extending between the cells and reading and writing circuitry, inherently taught by the reference, since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type, which include word lines and data lines to process the charge stored, an electrically insulating layer (6) on the substrate, a charge storage node (7), an electrode (11-2) forming part of the data lines and a barrier structure (8) between the electrode and the charge storage node and a control gate (9).

The limitations "*to read the level of charge stored on the charge storage nodes of the cells individually*", "*to write charge onto the charge storage nodes of the cells individually*" and "*the barrier structure providing a variable internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate being operable to receive an external voltage bias applied to one of the word lines so as to apply a field to the barrier structure resulting in a relatively low barrier height whereby a current flows through between the electrode and the memory node through the barrier structure so as to change the voltage on the memory node*", are intended use limitations which do not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 57, Hijiya teaches a substrate (1), a horizontal transistor (3, 4) formed I the substrate and a vertically configured controllable conduction device overlying the transistor

comprising a charge storage node (7), an electrode (11-2) forming part of the data lines and a barrier structure (8) between the electrode and the charge storage node and a control gate (9).

The limitation "*the barrier structure providing a variable internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate being operable to receive an external voltage bias applied to one of the word lines so as to apply a field to the barrier structure resulting in a relatively low barrier height whereby a current flows through between the electrode and the memory node through the barrier structure so as to change the voltage on the memory node*", is an intended use limitation which does not structurally distinguish the claimed limitation from that taught by Hijiya.

With regard to Claim 58, Hijiya teaches a substrate (1), an array of memory cells configured on the substrate and a plurality of word lines and data lines extending between the cells and reading and writing circuitry, inherently taught by the reference, since the disclosed structure is related to nonvolatile semiconductor memory device of the charge-storage type, which include word lines and data lines to process the charge stored, an electrically insulating layer (6) on the substrate, a charge storage node (7), an electrode (11-2) forming part of the data lines and a barrier structure (8) between the electrode and the charge storage node and a control gate (9).

The limitations "*to read the level of charge stored on the charge storage nodes of the cells individually*", "*to write charge onto the charge storage nodes of the cells individually*" and "*the barrier structure providing a variable internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate being operable to receive an external voltage bias applied to one of the word lines so as to apply a field to the barrier structure resulting in a relatively low barrier height whereby a current flows through between the electrode and the memory node through the barrier structure so as to change the voltage on the memory node*", are intended use limitations which do not structurally distinguish the claimed limitation from that taught by Hijiya.

Response to Arguments

3. Applicant's arguments with respect to claims 1-12, 15-34, 39-47 and 50-58 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on March 7, 2003 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 609(B)(2)(I). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

4/14/03

ALLAN R. WILSON
PRIMARY EXAMINER